WE CLAIM:

1. A method of verifying a full-chip electronic design of a programmable logic device (PLD) chip, the method comprising:

partitioning the PLD chip into a plurality of blocks;

generating a block level RTL model of one of the plurality of blocks;

generating a block level functional representation of the one of the plurality of blocks;

producing a full chip RTL model using the block level RTL model and the block level functional representation; and

using the full chip RTL model for verification, simulation or debugging.

2. The method of claim 1 wherein the programmable portion is partitioned into a plurality of rows and columns of logic array blocks (LABs).

3. The method of claim 1 wherein generating a block level RTL comprises:

creating a block level schematic of an electronic design;

extracting a block Ram Bit Address(RBA) file from the block level schematic;

extracting a block level CRAM array from the block level RBA file; and

generating the block level RTL using the block level CRAM array.

4. The method of claim 3 wherein the block level CRAM array comprises absolute coordinates and RAM bit values for each CRAM bit.

5. The method of claim 4 wherein the CRAM is EPROM, EEPROM, fuse, anti-fuse, SRAM, MRAM, FRAM, DRAM.

6. The method of claim 1 wherein generating a block level RTL comprises:

creating a block level schematic of an electronic design;

generating a full chip schematic using a plurality of the block level schematics;

producing a full chip RBA file from the full chip schematic;

extracting block level RBA file from the full chip RBA file;

extracting a block level CRAM array from the block level RBA file; and

generating a block level RTL model using the block level CRAM array.

7. The method of claim 6 wherein the block level CRAM array comprises absolute coordinates and RAM bit values for each CRAM bit.

8. The method of claim 7 wherein the CRAM is EPROM, EEPROM, fuse, anti-fuse, SRAM, MRAM, FRAM, DRAM.

9. The method of claim 1 further including:

comparing the block level RTL model to the block level schematic before producing a full chip RTL model; and

modifying the block level functional representation and the block level CRAM array if the block level RTL is not equivalent to the block level schematic.

10. The method of claim 1 wherein the PLD is a complex programmable logic device ("CPLD"), programmable array logic ("PAL"), programmable logic arrays ("PLA"), field PLA ("FPLA"), erasable PLDs ("EPLD"), electrically erasable PLD ("EEPLD"), logic cell arrays ("LCA") or field programmable gate arrays ("FPGA").

11. The method of claim 1 wherein the programmable logic device is embedded into another electronic device.

12. The method of claim 12 wherein the other electronic device comprises programmable and non-programmable circuitry.

13. The method of claim 2 wherein the LAB comprises a plurality of one or more of the following sub-blocks: LE, LIM, LAB wide, LEIM, CRAM and DIM.

14. The method of claim 1 wherein one or more of the plurality of blocks are digital signal processing blocks, input/output blocks, memory blocks, etc.

15. A data processing system for verifying a full-chip electronic design of a programmable logic device (PLD) chip, the data processing system including instructions for implementing the method of claim 1.

16. A method of verifying a programmable region of an electronic design, the method comprising:

partitioning the programmable region into a plurality of blocks;

generating a block level RTL model of one of the plurality of blocks;

generating a block level functional representation of the one of the plurality of blocks;

producing a full region RTL model from the block level RTL model and the block level functional representation; and

using the full region RTL model for verification, simulation or debugging.